Implementation of 5-Stage IEEE Single Precision Floating Point Adder

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The intension of the project to implement 5-state IEEE single precision (SP) floating point (FP) adder in:

1. Unpipelined design
2. Pipelined design

## I. Introduction

IEEE 754 is a technical standard describing computation of floating point number.

There are two representations of binary format, namely,

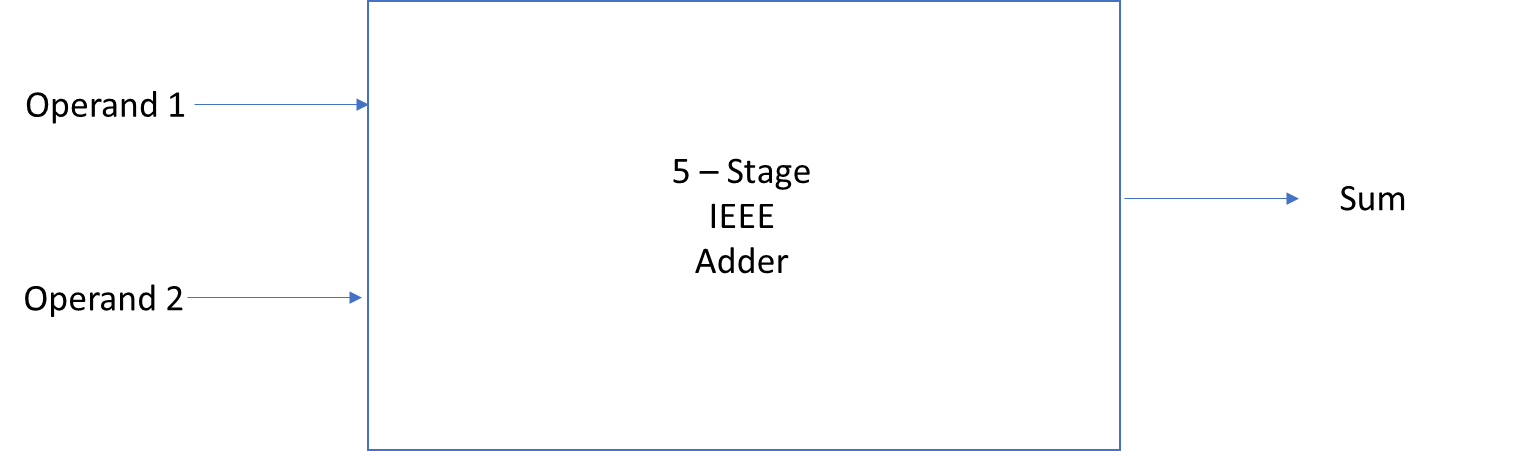
a. Single Precision: 32 bits

|  |  |  |
| --- | --- | --- |
| 1 sign bit | 8 bits for exponent | 23 bits for mantissa |

b. Double Precision: 64 bits

|  |  |  |
| --- | --- | --- |
| 1 sign bit | 11 bits for exponent | 53 bits for mantissa |

## Figure 1: IEEE 5-stage adder block diagram



## Table 2: List of Test Case

|  |  |  |
| --- | --- | --- |
| **Test Case** | **Operand 1** | **Operand 2** |
| 1. | 98 | -169 |
| 2. | 99 | -89 |
| 3. | -45 | 79 |
| 4. | -283 | -66 |
| 5. | 0 | 0 |
| 6. | 0 | -117 |
| 7. | -110.125 | 99.875 |
| 8. | 110.875 | 99.125 |

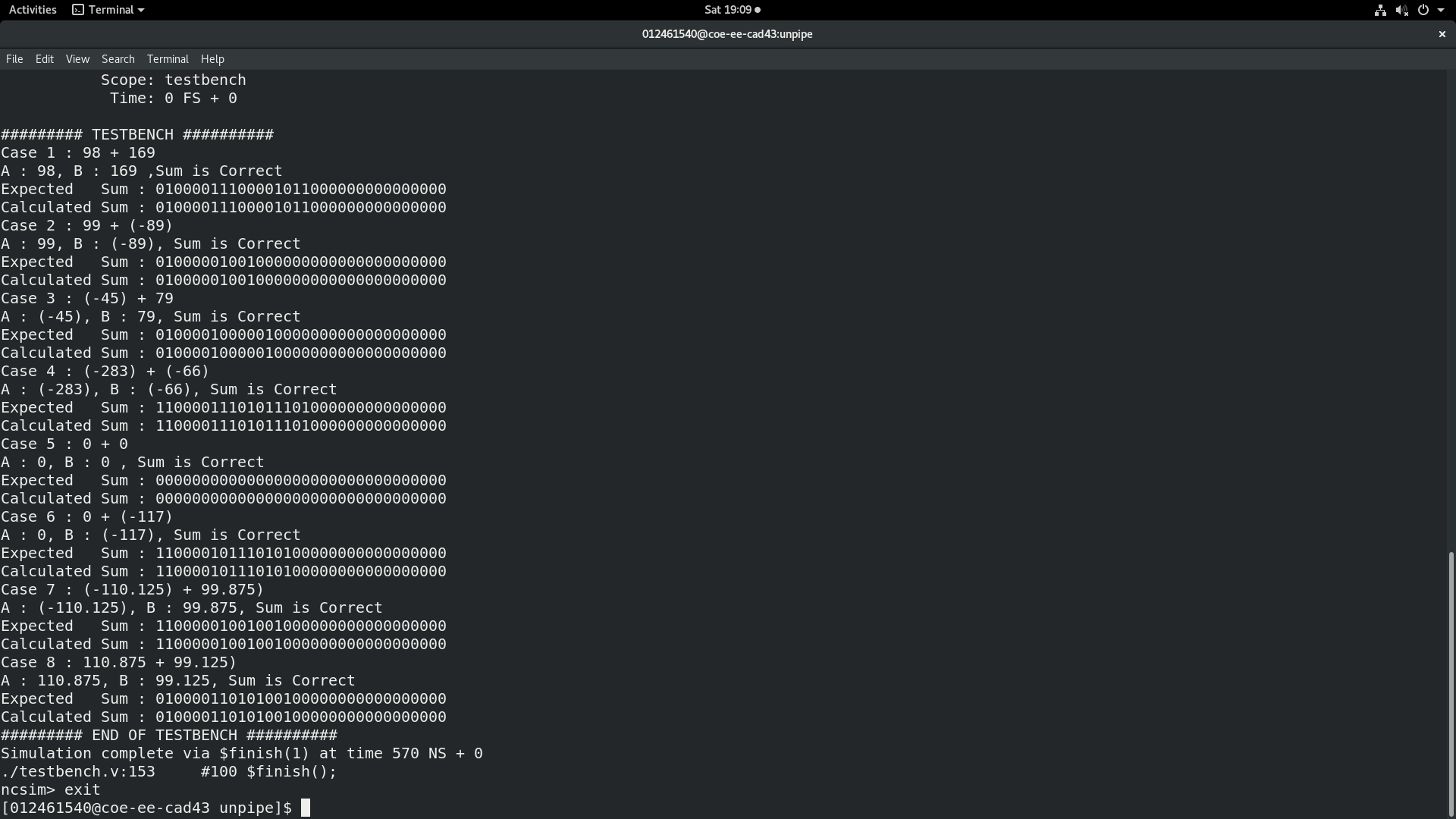
## II. Description

The 5-stage addition of floating point is defined as following flow chart:

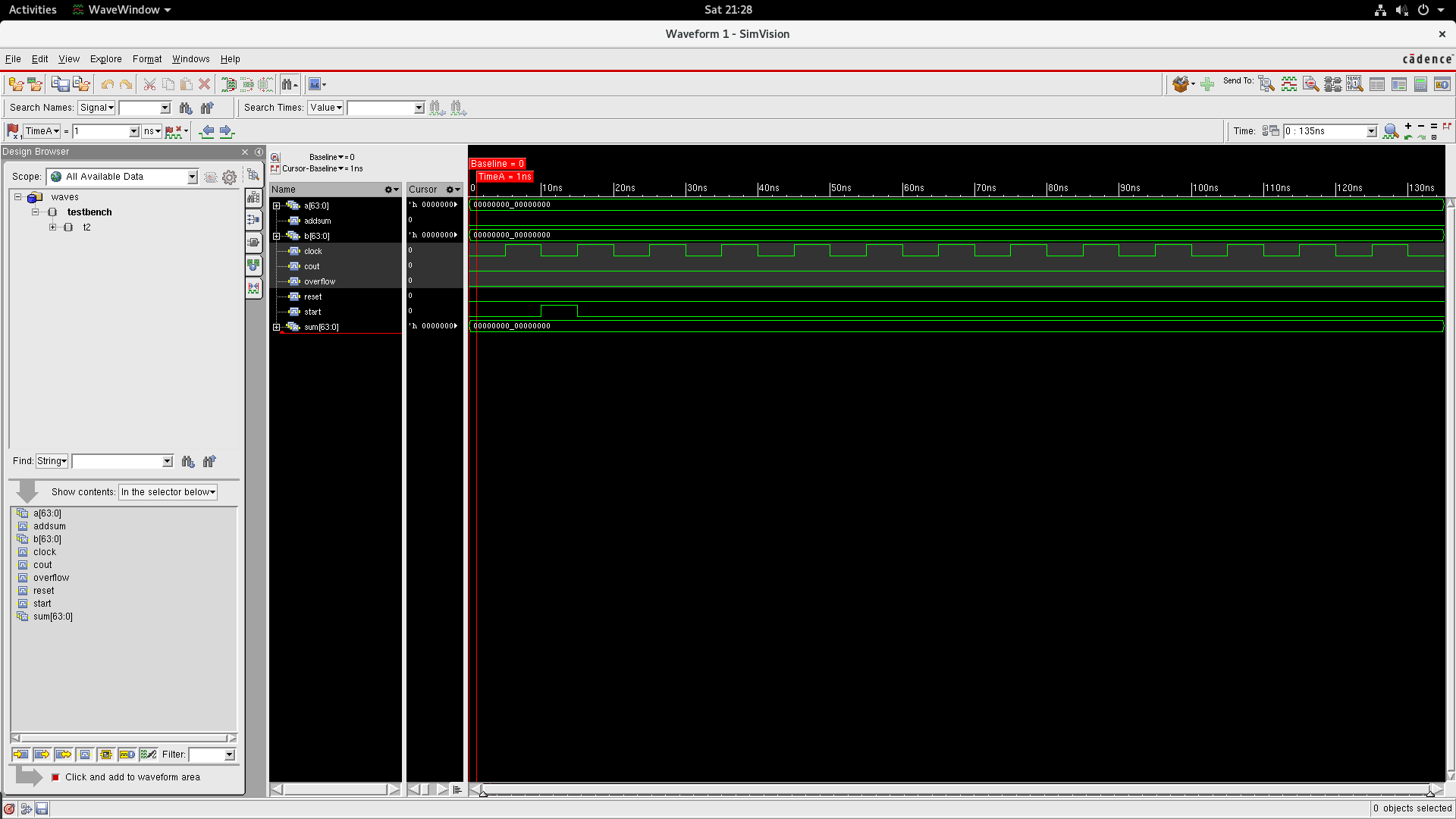
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## III. Simulation and Verification Results

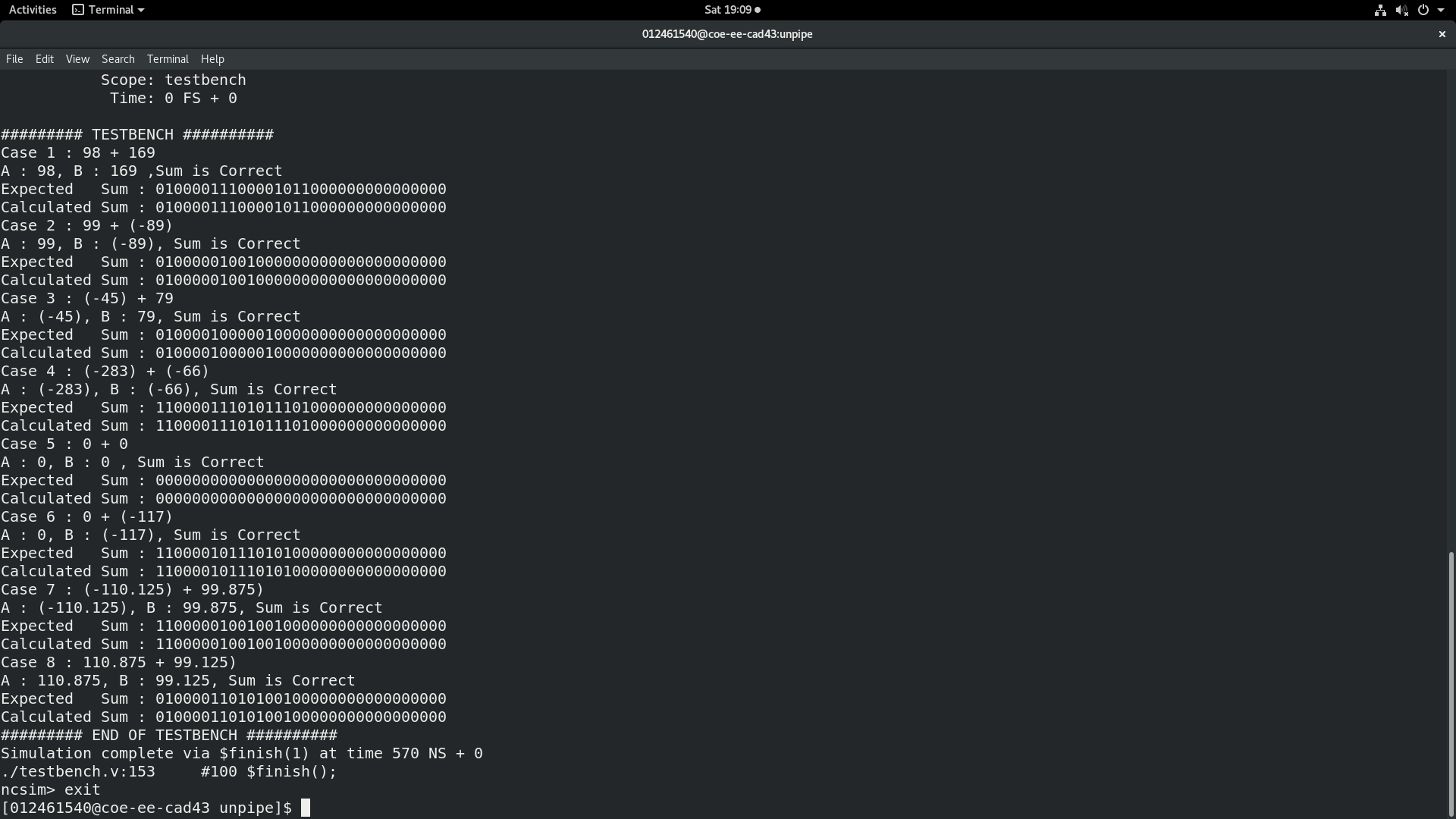
**Figure III.a**: Simulation Log that contains unpipelined design



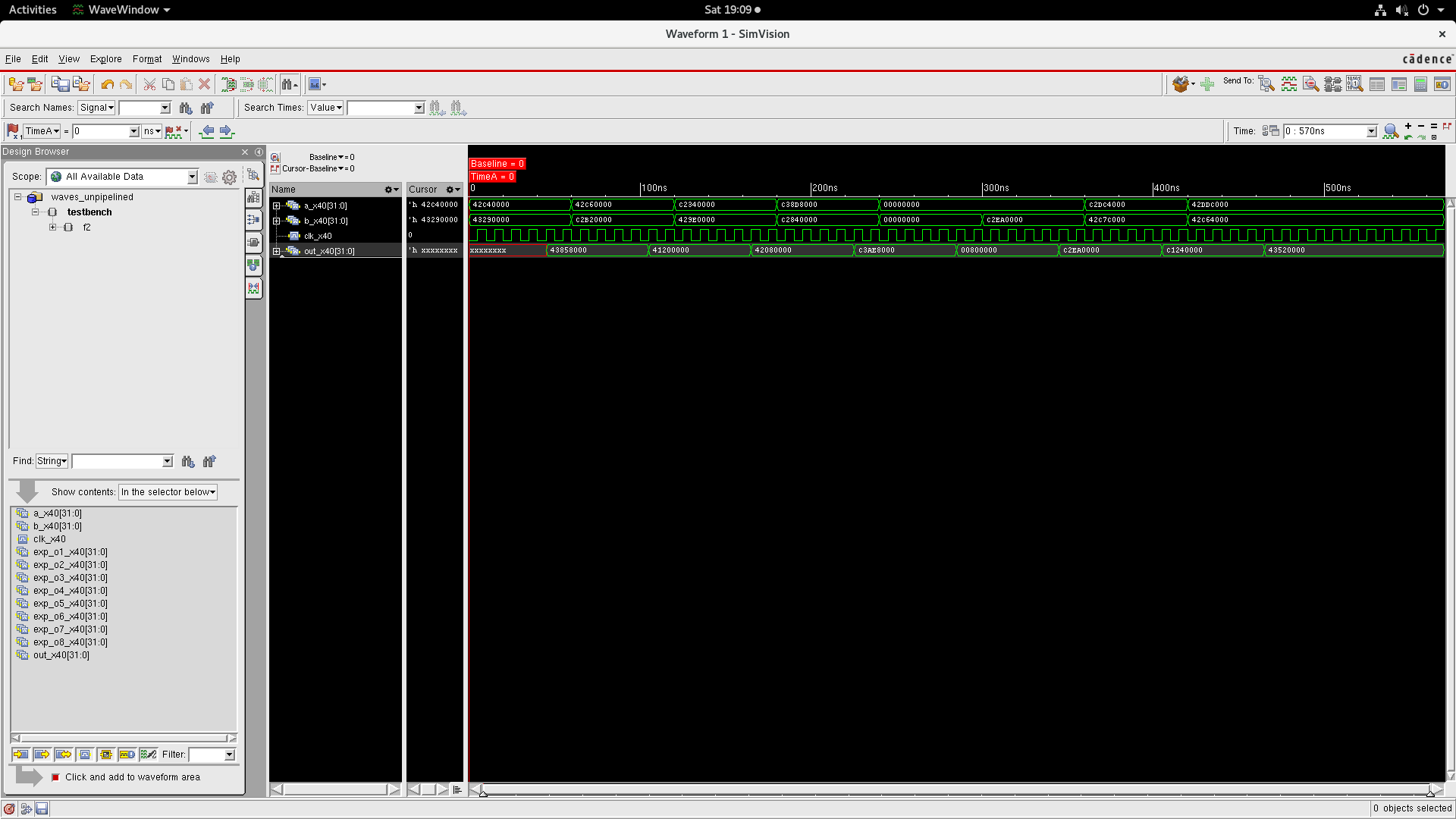
**Figure III.b**: RTL simulation waveform that contains unpipelined design



**Figure III.c**: Simulation Log that contains unpipelined design



**Figure III.d**: RTL simulation waveform that contains unpipelined design



## Conclusion

Successfully implemented single precision floating pint adder complying to IEEE standard. All given testcases passed in pipelined and unpipelined design.